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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,023	11/27/2001	Andrew Mark Nightingale	550-286	1196

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EXAMINER	
ALHIJA, SAIF A	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,023	NIGHTINGALE, ANDREW MARK	
	Examiner	Art Unit	
	Saif A. Alhija	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-12,14-22 and 24-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-12,14-22 and 24-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-2, 4-12, 14-22, and 24-30 have been presented for examination.

Response to Arguments

2. Applicant's arguments filed 10 May 2006 have been fully considered but they are not persuasive.

i) Applicant argues that the Examiner maintained the non-statutory subject matter rejection of claim 21 following Applicant amendment of the claim. The Examiner points out that the claim was rejected for being in improper form for the representation for code. Following Applicants amendment the 101 rejection of claim 21 has been withdrawn.

ii) The Applicants Attorney is discussing a technological arts rejection which was not made. Applicants statements appear to question the validity of US Patents. Applicants provided hypothetical conclusory arguments regarding issued patents. Examiner will not address said arguments.

iii) Claims 1 and 11 were rejected under 35 U.S.C. 101 because the claimed invention appeared to be directed to non-statutory subject matter. The Examiner asserted that the current state of the claim language is such that a reasonable interpretation of the claims would not result in any useful, concrete or tangible result. The Examiner asserted that the claims do not indicate if the methods or apparatus are tangible methods or apparatus in the form of hardware, instead of an arrangement of software lacking tangible embodiment. A hardware simulator, signal interface controller, and test scenario manager can be defined by a broadest reasonable interpretation to be either a hardware element or a software element. Therefore, if these elements are interpreted to be software then the claims constitute an arrangement of software lacking tangible embodiment. However, since the Applicant has pointed out that the elements of the claim are hardware, the 35 U.S.C. 101 rejections have been withdrawn.

iv) Applicant argues that the reference does not disclose "wherein said test scenario manager includes a shared data memory into which a signal interface controller may store data using a test scenario controlling message sent from said signal interface controller to said test scenario manager, said data

being readable from said shared data memory by at least one of: (i) another signal interface controller; " However, as per Column 7, Line 60 – Column 8 Line 5 as well as Figure 5 the control CPU's are connected to the Main System CPU as well as each other in order to allow for data transfer, synchronization, etc. Therefore since the verification units are connected to Control CPU and the Standard Bus, there is a connection between the elements and allows communication between them for situations of arbitration, synchronization, etc. Therefore the rejection is maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. **Claim(s) 1-2, 4-12, 14-22, and 24-30** are rejected under 35 U.S.C. 102(e) as being clearly anticipated by **Rajsuman et al. "Method and Apparatus for SOC Design Validation" U.S. Patent 6,678,645.**

Regarding Claims 1, 11, and 21

Rajsuman et al. discloses an apparatus, method, and computer program product embodied on a computer-readable medium and comprising code that when executed controls a computer for simulating data processing operations performed by a data processing apparatus, said apparatus comprising:

a hardware simulator responsive to one or more stimulus signals to generate one or more response signals simulating a response of said data processing apparatus to said one or more stimulus signals if applied to said data processing apparatus; **(Column 5, Lines 41-48)**

a plurality of signal interface controllers **(labeled as Verification Unit in Rajsuman et al.)** coupled to said hardware simulator, each signal interface controller serving to perform one or more simulation actions transferring at least one of one or more stimulus signals and one or more response signals between a corresponding portion of said hardware simulator and said signal interface controller as part of simulating said data processing operations; **(Column 5, Lines 43-44)** and

a test scenario manager coupled to said plurality of signal interface controllers and operable to transfer test scenario controlling messages to said plurality of signal interface controllers, at least one of said test scenario controlling messages including: **(Column 5, Lines 32-34)**

(i) data defining a simulation action to be performed by a signal interface controller; and **(Column 5, Lines 32-38)**

(ii) data defining when said signal interface controller should perform said simulated action. **(Column 10, Lines 25-26)**

wherein said test scenario manager includes a shared data memory into which a signal interface controller may store data using a test scenario controlling message sent from said signal interface controller to said test scenario manager, said data being readable from said shared data memory by at least one of:

(i) another signal interface controller; **(Column 7, Line 60 – Column 8 Line 5. Figure 5)**

Regarding Claims 2, 12, and 22

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 1, 11, and 21 respectively; wherein said data defining when said signal interface controller should perform said simulated action includes at least one of:

(i) a time value; **(Column 10, Lines 25-26)**

(ii) a delay value; and

(iii) a value specifying said simulated action should be performed when a specified event is simulated as occurring. **(Column 10, Lines 35-36)**

Regarding Claims 4, 14, and 24

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 1, 11, and 21 respectively; wherein a first signal interface controller is responsive to simulation results captured by a second signal interface controller, written to said shared data memory by said second signal interface controller and then read from said shared data memory by said first signal interface controller. **(Column 8, Lines 2-5, and Figure 6, Elements 671-676, 76, and 661-665)**

Regarding Claims 5, 15, and 25

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 1, 11, and 21 respectively; wherein said hardware simulation is simulated using software running upon a general purpose computer. **(Column 5, Lines 32-34)**

Regarding Claims 6, 16, and 26

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 1, 11, and 21 respectively; wherein each signal interface controller includes an action queue of simulation actions to be performed by said signal interface controller. **(Column 8, Lines 13-15)**

Regarding Claims 7, 17, and 27

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 6, 16, and 26 respectively; wherein each signal interface controller includes a test scenario manager

interface operable to exchange test scenario controlling messages with said test scenario manager and to add simulation actions to said action queue. **(Column 8, Lines 6-9, and 13-15)**

Regarding Claims 8, 18, and 28

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 6, 16, and 26 respectively; wherein each signal interface controller includes a peripheral interface operable to transform simulation actions specified in said action queue into signal values exchanged with said hardware simulation. **(Column 6, Lines 62-63)**

Regarding Claims 9, 19, and 29

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 1, 11, and 21 respectively; wherein test scenario manager sends a machine generated sequence of simulation actions to said plurality of signal interface controllers to perform random simulation testing of said data processing apparatus. **(Column 2, Lines 31-32)**

Regarding Claims 10, 20 and 30

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 1, 11, and 21 respectively; wherein said test scenario manager is operable as a master device and said plurality of signal interface controllers are operable as slave devices to said master device. **(Column 13, Lines 7-10)**

Conclusion

4. Applicant's arguments filed **10 May 2006** have been fully considered but they are not persuasive therefore **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. All Claims are rejected.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

July 6, 2006

KAMINI SHAH
SUPERVISORY PATENT EXAMINER